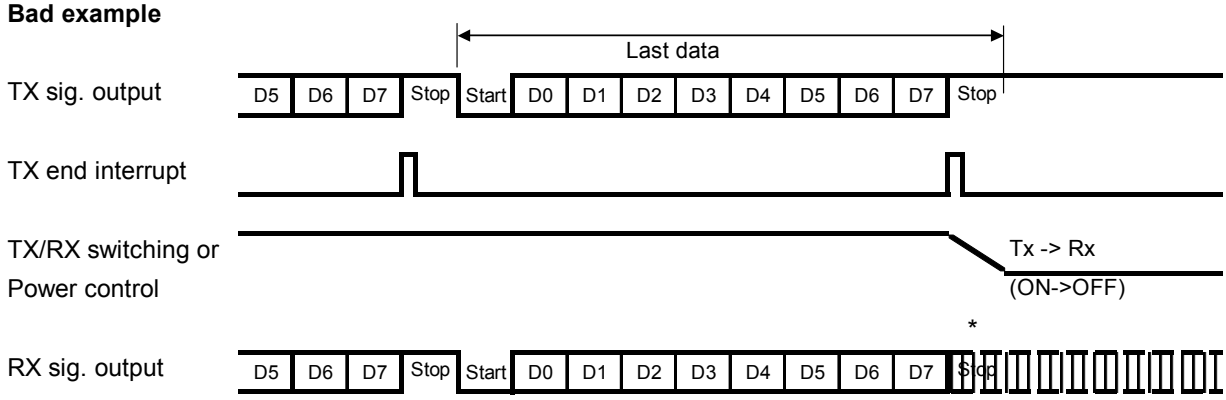
Notes for radio module control using a CPU

When using a CPU to control the radio module and output the transmission signal using a serial interface like SIO or UART, the following points should be noted.

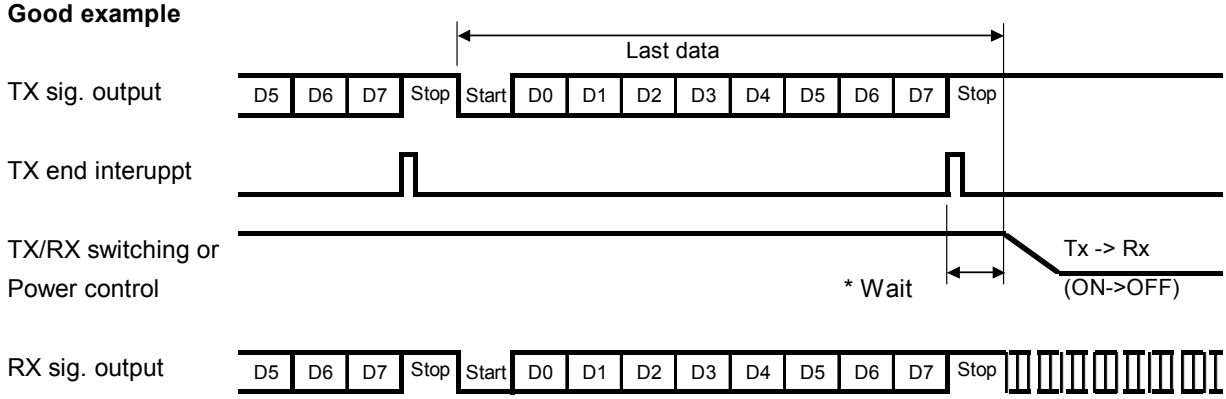
In general, an interrupt that indicates the end of the transmission is generated when the data to be sent is set in the shift register in CPU. The point where the interrupt is generated occurs before output of the last bit is completed. (Some CPUs that have double buffers in the transmitter part generate the interrupt earlier).
Because of this, when operating the radio module immediately after the interrupt such as turning the power off or switching TX to RX, the last bit to be transmitted may be corrupted, or even if the bit is not corrupted, sufficient transmission range may not be obtained due to loss of power. Therefore the user is urged to check the operation manual of the CPU to be used or check the transmission signal with an oscilloscope to ensure a sufficient interval before issuing controls for power and/or TX/RX switching.
Timing examples when UART is used are shown below. Here, an interrupt is generated at the same time as the start of the stop bit is being output in the CPU.

Bad example



* Transmitting is turned off before the last bit (stop bit) is transmitted, therefore the bit might result in an error at the receiver side.

Good example



* In this example, the CPU waits for 1 bit or more and completes the transmission of the last bit, then turns the power of the radio module off.