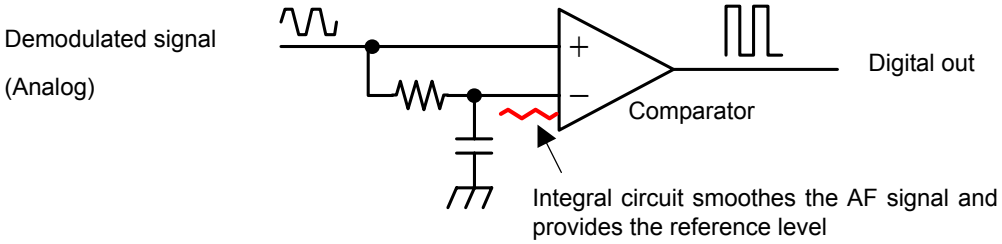
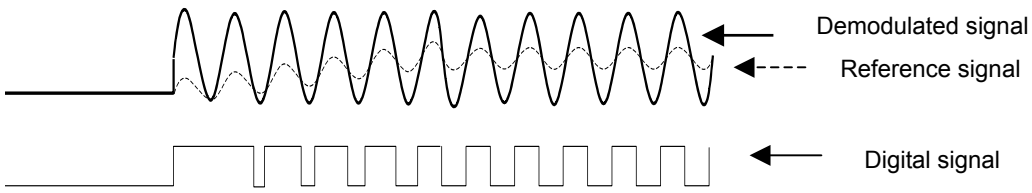
Data demodulation in CDP-RX-03AS/BS

Slicer circuit

The AF output signal (analogue) from the demodulation IC is converted to digital signal by the comparator in the CDP-RX-03AS/BS.
Since the DC level of the AF output varies along with the frequency variation of the transmitter and/or receiver, the electronic circuit below is basically used for smoothing the AF output signal and for providing the reference level of the comparator.

A signal communication format like NRZ includes a long period of no transition from high to low that is often called long low and long high state. The time constant of the integral circuit in the CDP-RX-03AS/BS is set slow at several tens of milliseconds so that the fixed period of long low/high state can be digitized correctly.
However, this results in a delay before the reference level of comparator reaches the optimal level just after the receiver gets the signal, and also it takes a long time for the duty cycle of the digital data out pulse to become stable.





Measurement data

The results of AF and DATA output signal measurement are shown below. While no signal is transmitted from the transmitter, the receiver demodulates the noise (field noise). When the CDP-RX-03AS receives the signal at this point, optimizing the reference level of comparator takes a while.
The data rate effects the amount of time required for the duty cycle of the digital data output pulse to become stable. When the data rate is 4,800 bps, it takes approximately 50 ms (with a 1010… repeated signal).
Therefore it is recommended to transmit a 1010.. repeated preamble for more than 50 ms in front of the user data when the transmitter starts transmission.

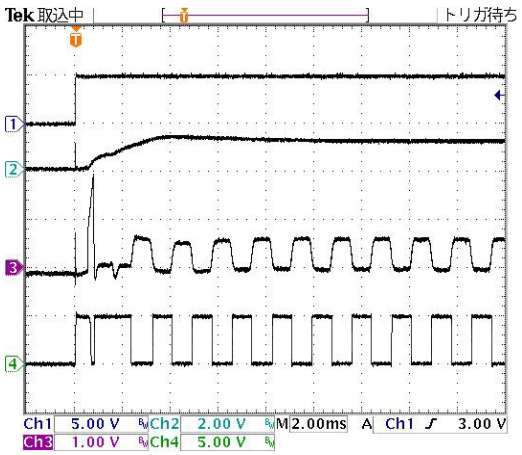
If the signal communication format carries coding like Manchester coding to avoid continuous long low / long high state in the signal, it is possible to shorten the time required for the duty cycle of the data output pulse to become stable by connecting a comparator circuit like the one above to the AF output terminal of CDP-RX-03AS externally for digitalization and optimizing the time constant of the integral circuit.

Measurement result
TX (Transmitter): CDP-TX-04S 869.75MHz RX (Receiver): CDP-RX-03AS 869.75MHz
Signal: 1010.. repeated

CH1: Power for both TX and RX
CH2: RX RSSI output
CH3: RX AF output
CH4: RX DATA output

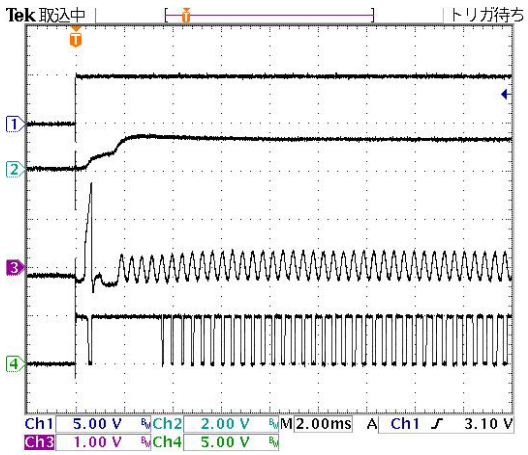
< The power of both TX and RX are ON at the same time >

Data rate: 1,200 bps



Start up

Data rate: 4,800 bps

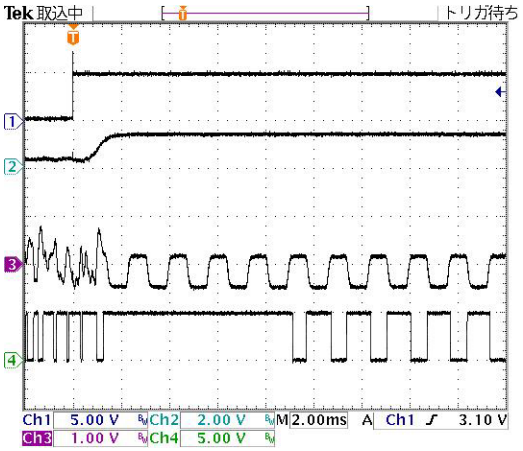


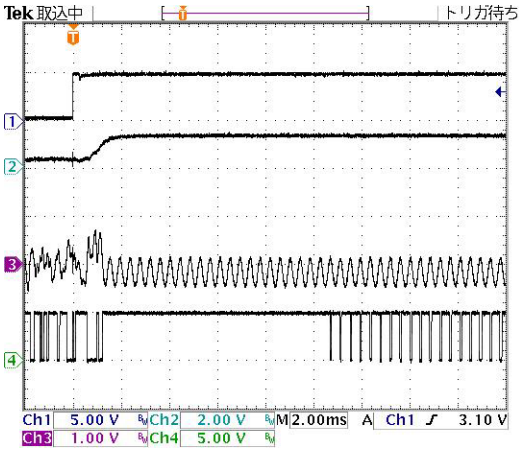
< RX power left ON, only TX power is turned on >

Signal: 1,200 bps

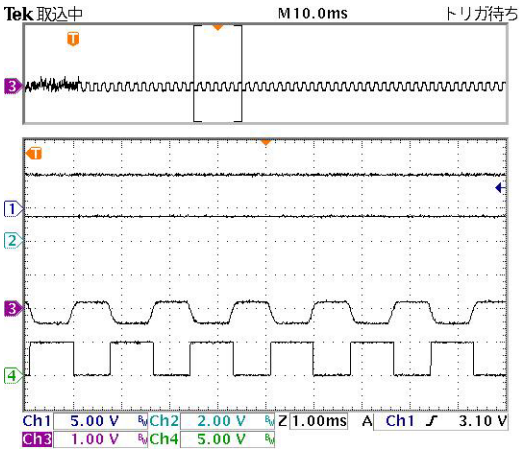
Signal: 4,800 bps

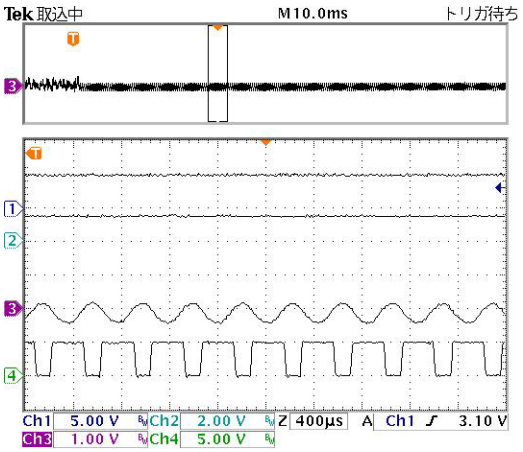
Start up





30 ms after start up





50 ms after start up