

UHF Narrow band radio transceiver **STD-302N-R 335 MHz**



Operation Guide

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GENERAL DESCRIPTION & FEATURES

General Description

The UHF FM narrow band semi-duplex radio data module STD-302N-R is a high performance transceiver designed for use in industrial applications requiring long range, high performance and reliability.

All high frequency circuits are enclosed inside a robust housing to provide superior resistance against shock and vibration. A narrow band technique enables high interference rejection and concurrent operation with multiple modules.

STD-302N-R, a narrowband module with 25 kHz channel steps, achieves high TX/RX switching speed, making it an ideal RF unit for inclusion in feedback systems.

Features

- 1 mW RF power, 3.0 V operation
- Programmable RF channel
- Fast TX/RX switching time
- High sensitivity -120 dBm
- Excellent mechanical durability, high vibration & shock resistance

Applications

- Telemetry
 - Water level monitor for rivers, dams, etc.
 - Monitoring systems for environmental data such as temperature, humidity, etc.
 - Transmission of measurement data (pressure, revolution, current, etc) to PC
 - Security alarm monitoring
- Telecontrol
 - Industrial remote control systems
 - Remote control systems for factory automation machines
 - Control of various driving motors
- Data transmission
 - RS232/RS485 serial data transmission

Note: In India, license-exempt application allocated in the 335 MHz band is only remote control systems of cranes.

SPECIFICATIONS

STD-302N-R 335 MHz

* The MIN/TYP/MAX values for the RF output power and BER are specified in the range of operation environment temperature.

* All values in the Specification column are specified at 25 °C +/- 10 °C unless otherwise noted.

General characteristics

Item	Units	MIN	TYP	MAX	Remarks
Communication method		One way, Half-duplex			
Emission class		F1D			
Operating frequency range	MHz	335.7125		335.8375	
Operation temperature range	°C	-20		60	No dew condensation
Storage temperature range	°C	-30		75	No dew condensation
Aging rate (/ year)	ppm	-1		1	TX freq., RX Lo freq.
Initial frequency tolerance *	ppm	-1.5		1.5	TX freq., RX Lo freq. At delivery
Dimensions	mm	30 x 50 x 9 mm			Not including protrusion
Weight	g	25 g			

* Initial frequency tolerance: At delivery

Initial frequency tolerance is defined as frequency drift at delivery within 1 year after the final adjustment

Electrical specification <Common>

Item		MIN	TYP	MAX	Remarks
Oscillation type		PLL controlled VCO			
Frequency stability (-20 to 60°C)	ppm	-4		4	Reference frequency at 25 °C
TX/RX switching time	ms		15	20	DI/DO
Channel step	kHz		25		
Data rate	bps	2400		4800	DO/DI
Max. pulse width	ms		15	20	DO/DI
Min. pulse width	us	200			DO/DI
Data polarity		Positive			DO/DI
PLL reference frequency	MHz		21.25		TCXO
PLL response	ms		30	60	from PLL setting to LD out
Antenna impedance	Ω		50		Nominal
Operating voltage	V	3.0		5.5	
TX consumption current	mA		38	42	Vcc = 3.0 V
RX consumption current	mA		26	30	Vcc = 3.0 V

For the PLL interface, refer to the documents of MB15E03SLP (FUJITSU) and use it within the specifications

Transmitter part

Item		MIN	TYP	MAX	Remarks
RF output power	mW	0.5	1	3	Conducted 50 Ω
Deviation	kHz	+/- 2.1	+/- 2.4	+/- 2.7	PN9 4800 bps
DI input level	V	0		5.5	L= GND, H = 3 V- Vcc
Residual FM noise	kHz		0.17		DI=L, LPF=20 kHz
Spurious emission	dBm		-54		Conducted 50Ω
Adjacent CH power	dBm	-	-37		PN9 4800 bps CH25 kHz/BW 10 kHz
Occupied bandwidth	kHz			10	PN9 4800 bps

Receiver part

Item		MIN	TYP	MAX	Remarks
Receiver type		Double superheterodyne			
1st IF frequency	MHz		21.7		
2nd IF frequency	kHz		450		
Maximum input level	dBm			10	
BER (0 error/2556 bits) ^{*1}	dBm	-108	-117		PN 9 4800 bps
BER (1 % error) ^{*2}	dBm		-120		PN 9 4800 bps
Sensitivity 12dB/ SINAD	dBm		-120		fm1 k/ dev 2 kHz CCITT
Spurious response rejections ^{*3}	dB		70		1 st Mix, 2 signal method, 1 % error
			55		2 nd Mix, 2 signal method, 1 % error
Adjacent CH selectivity ^{*3}	dB		50		+/- 25 kHz, 2 signal method, 1 % error
Blocking	dB		84		Jamming signal +/- 1MHz, 2 signal method, 1% error
Intermodulation ^{*4}	dB		50		2 signal method, 1 % error
DO output level	V	0		2.8	L = GND H = 2.8 V
RSSI rising time	ms		30	50	CH shift of 25 kHz (from PLL setup)
			50	100	When power ON (from PLL setup)
Time until valid Data-out ^{*5}	ms		50	70	CH shift of 25 kHz (from PLL setup)
			70	120	When power ON (from PLL setup)
Spurious radiation (1 st Lo)	dBm		-57		Conducted 50 Ω
RSSI	mV	300	360	420	With -97 dBm at 335.7875 MHz
		190	250	310	With -113 dBm at 335.7875 MHz

Specifications are subject to change without prior notice

Notice

- Communication range depends on the operation environment and ambient surrounding
- Specifications are subject to change to improve the characteristics and for other reasons.
- The time required until a stable DO is established may get longer due to the possible frequency drift caused by operation environment changes, especially when switching from TX to RX, from RX to TX and changing channels. Please make sure to optimize the timing. The recommended preamble is more than 20 ms.
- Antenna connection is designed as pin connection. RF output power, sensitivity, spurious emission and spurious radiation levels may vary with the pattern used between the RF pin and the coaxial connection. Please make sure to verify those parameters before use.
- The feet of the shield case should be soldered to the wide GND pattern to avoid any change in characteristics.

Notes about the specification values

*1 BER: RF level where no error per 2556 bits is confirmed with the signal of PN9 and 4800 bps.

*2 BER (1 % error): RF level where 1% error per 2556 bits is confirmed with the signal of PN9 and 4800 bps.

*3 Spurious response, CH selectivity, Blocking: Jamming signal used in the measurement is unmodulated.

*4 Intermodulation: Ratio between the receiver input level with BER 1% and the signal level (PN9 4800 bps) added at the points of 'Receiving frequency - 200 kHz' + 'Receiving frequency -100kHz' with which BER 1% is achieved.

*5 Time until valid Data-out: Valid DO is determined at the point where Bit Error Rate meter starts detecting the signal of 4800 bps, 1010 repeated signal.

All specifications are specified based on the data measured in a shield room using the PLL setting controller board prepared by Circuit Design.

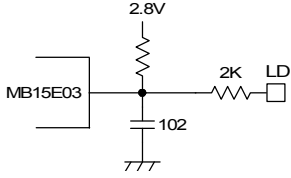
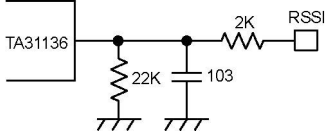
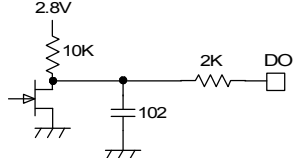
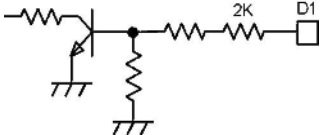
Measuring equipment:

SG=ANRITSU communication analyzer MT2605

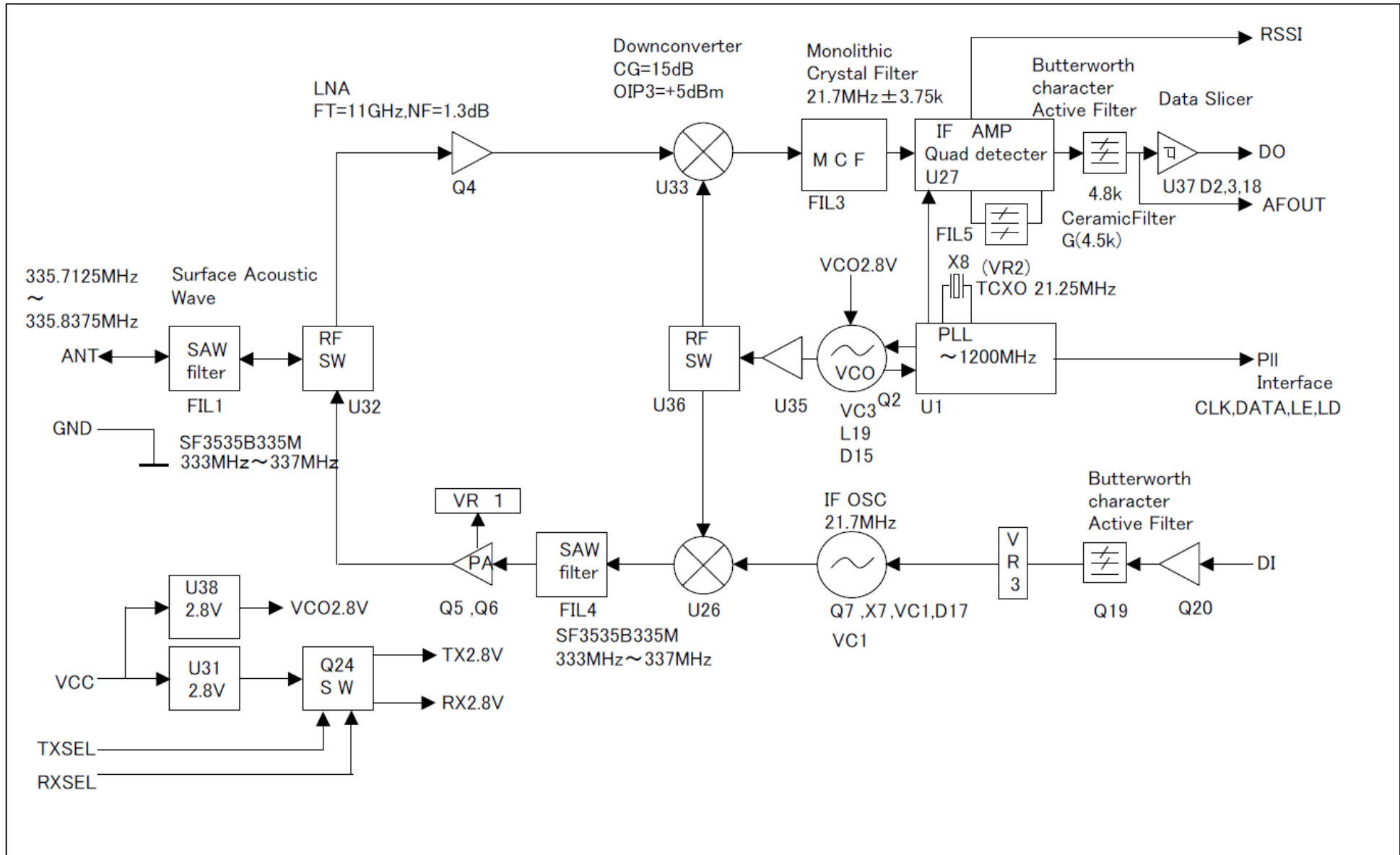
Spectrum analyzer = ANRITSU MS2663G / BER measure = ANRITSU MP1201G

PIN DESCRIPTION

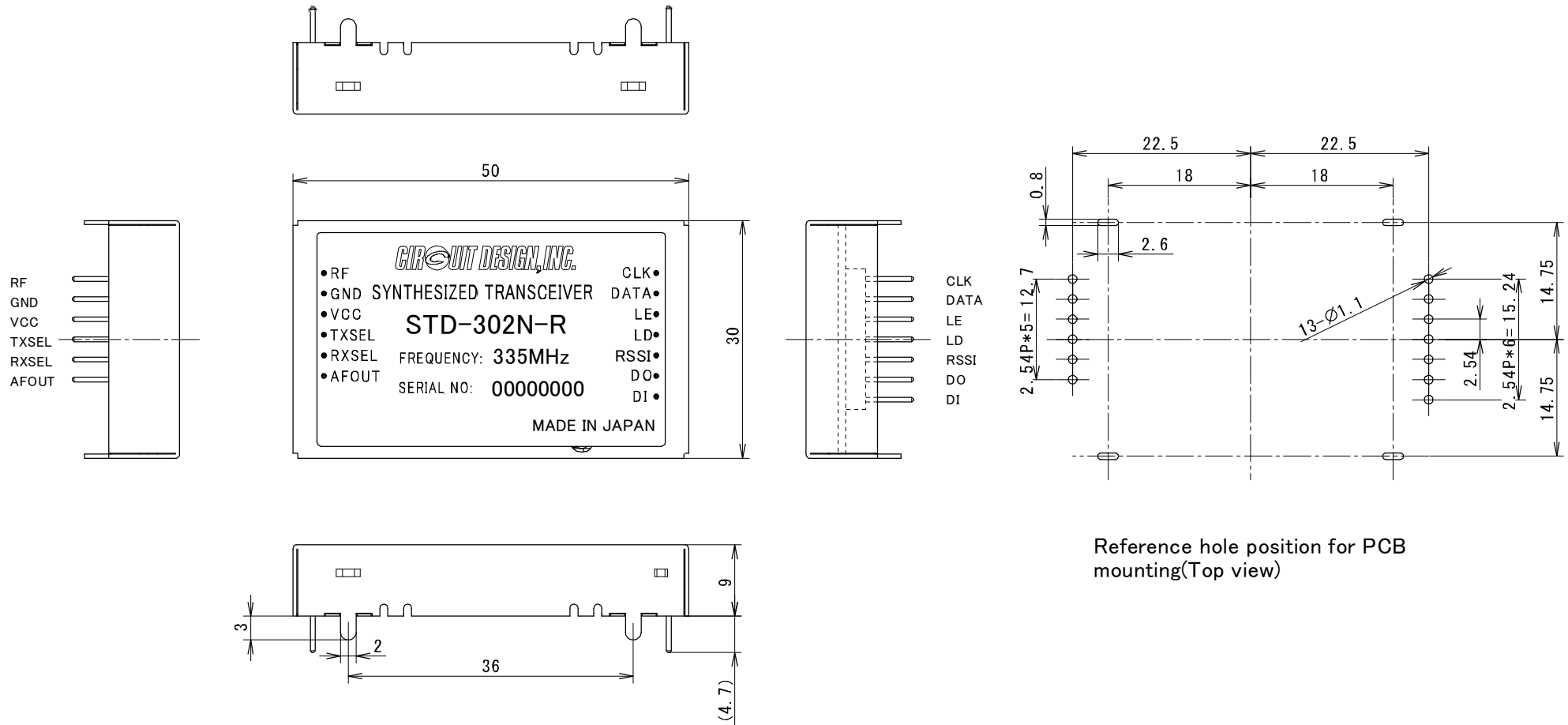
Pin name	I/O	Description	Equivalent circuit
RF	I/O	RF input terminal Antenna impedance nominal 50 Ω	
GND	I	GROUND terminal The GND pins and the feet of the shield case should be connected to the wide GND pattern.	
VCC	I	Power supply terminal DC 3.0 to 5.5 V	
TXSEL	I	TX select terminal GND = TXSEL active To enable the transmitter circuits, connect TXSEL to GND and RXSEL to OPEN or 2.8 V.	
RXSEL	I	RX select terminal GND= RXSEL active To enable the receiver circuits, connect RXSEL to GND and TXSEL to OPEN or 2.8 V.	
AF	I	Analogue output terminal There is DC offset of approx. 1 V. Refer to the specification table for amplitude level.	
CLK	I	PLL data setting input terminal Interface voltage H = 2.8 V, L = 0 V	
DATA	I	PLL data setting input terminal Interface voltage H = 2.8 V, L = 0 V	
LE	I	PLL data setting input terminal Interface voltage H = 2.8 V, L = 0 V	

LD	O	PLL lock/unlock monitor terminal Lock = H (2.8 V), Unlock = L (0 V)	
RSSI	O	Received Signal Strength Indicator terminal	
DO	O	Data output terminal Interface voltage: H=2.8V, L=0V	
DI	I	Data input terminal Interface voltage: H=2.8V to Vcc, L=0V Input data pulse width Min. 100 μs Max. 15 ms	

BLOCK DIAGRAM <STD-302N-R 335 MHz>

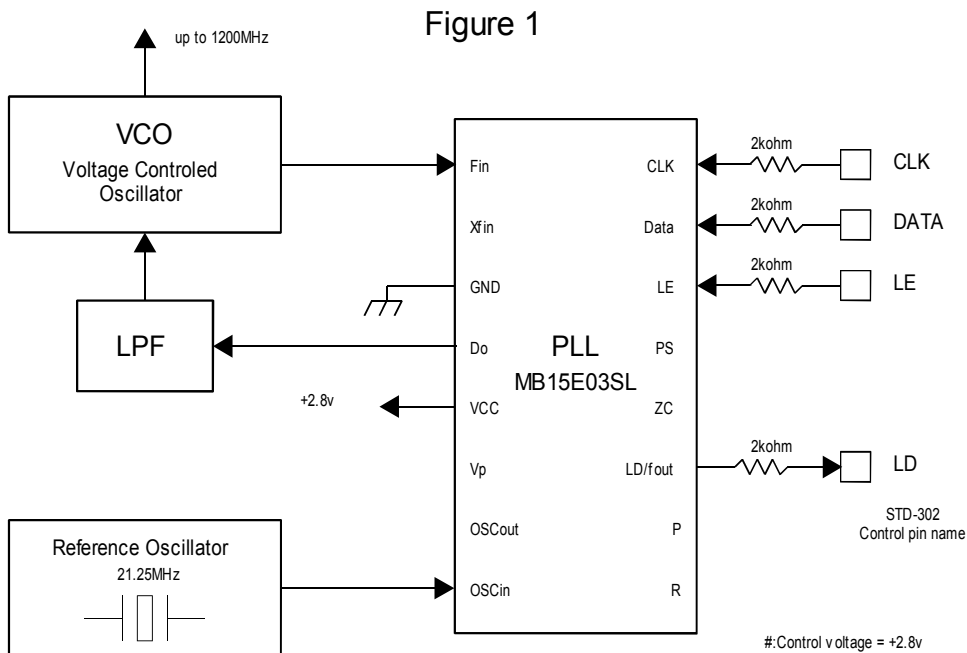


DIMENSIONS



PLL IC CONTROL

● **PLL IC control**



STD-302N-R is equipped with an internal PLL frequency synthesizer as shown in Figure 1. The operation of the PLL circuit enables the VCO to oscillate at a stable frequency. Transmission frequency is set externally by the controlling IC. STD-302N-R has control terminals (CLK, LE, DATA) for the PLL IC and the setting data is sent to the internal register serially via the data line. Also STD-302N-R has a Lock Detect (LD) terminal that shows the lock status of the frequency. These signal lines are connected directly to the PLL IC through a 2 kΩ resistor.

The interface voltage of STD-302N-R is 2.8 V, so the control voltage must be the same. STD-302N-R comes equipped with a Fujitsu MB15E03SL PLL IC. Please refer to the manual of the PLL IC.

The following is a supplementary description related to operation with STD-302N-R. In this description, the same names and terminology as in the PLL IC manual are used, so please read the manual beforehand.

● How to calculate the setting values for the PLL register

The PLL IC manual shows that the PLL frequency setting value is obtained with the following equation.

$$f_{vco} = [(M \times N) + A] \times f_{osc} / R \quad \text{--- Equation 1}$$

f_{vco} : Output frequency of external VCO

M: Preset divide ratio of the prescaler (64 or 128)

N: Preset divide ratio of binary 11-bit programmable counter (3 to 2,047)

A: Preset divide ratio of binary 7-bit swallow counter ($0 \leq A \leq 127$ $A < N$)

f_{osc} : Output frequency of the reference frequency oscillator

R: Preset divide ratio of binary 14-bit programmable reference counter (3 to 16,383)

With STD-302N-R, there is an offset frequency (f_{offset}) 21.7 MHz for the transmission RF channel frequency f_{ch} . Therefore the expected value of the frequency generated at VCO (f_{expect}) is as below.

$$f_{vco} = f_{expect} = f_{ch} - f_{offset} \quad \text{--- Equation 2}$$

The PLL internal circuit compares the phase to the oscillation frequency f_{vco} . This phase comparison frequency (f_{comp}) must be decided. f_{comp} is made by dividing the frequency input to the PLL from the reference frequency oscillator by reference counter R. STD-302N-R uses 21.25 MHz for the reference clock f_{osc} . f_{comp} is one of 6.25 kHz, 12.5 kHz or 25 kHz.

The above equation 1 results in the following with $n = M \times N + A$, where “n” is the number for division.

$$f_{vco} = n \times f_{comp} \quad \text{--- Equation 3} \quad n = f_{vco} / f_{comp} \quad \text{--- Equation 4} \quad \text{note: } f_{comp} = f_{osc} / R$$

Also, this PLL IC operates with the following R, N, A and M relational expressions.

$$R = f_{osc} / f_{comp} \quad \text{--- Equation 5} \quad N = \text{INT}(n / M) \quad \text{--- Equation 6} \quad A = n - (M \times N) \quad \text{--- Equation 7}$$

INT: integer portion of a division.

As an example, the setting value of RF channel frequency f_{ch} 869.725 MHz can be calculated as below.

The constant values depend on the electronic circuits of STD-302N-R.

Conditions:	Channel center frequency:	$f_{ch} = 869.725$ MHz
	Constant: Offset frequency:	$f_{offset} = 21.7$ MHz
	Constant: Reference frequency:	$f_{osc} = 21.25$ MHz
	Set 25 kHz for Phase comparison frequency and 64 for Prescaler value M	

The frequency of VCO will be

$$f_{vco} = f_{expect} = f_{ch} - f_{offset} = 869.725 - 21.7 = 848.025 \text{ MHz}$$

Dividing value “n” is derived from Equation 4

$$n = f_{vco} / f_{comp} = 848.025 \text{ MHz} / 25 \text{ kHz} = 33921$$

Value “R” of the reference counter is derived from Equation 5.

$$R = f_{osc} / f_{comp} = 21.25 \text{ MHz} / 25 \text{ kHz} = 850$$

Value “N” of the programmable counter is derived from Equation 6.

$$N = \text{INT}(n / M) = \text{INT}(33921 / 64) = 530$$

Value “A” of the swallow counter is derived from Equation 7.

$$A = n - (M \times N) = 33921 - 64 \times 530 = 1$$

The frequency of STD-302N-R is locked at a center frequency f_{ch} by inputting the PLL setting values N, A and R obtained with the above equations as serial data. The above calculations are the same for the other frequencies.

Excel sheets that contain automatic calculations for the above equations can be found on our web site (www.circuitdesign.jp/eng/).

The result of the calculations is arranged as a table in the CPU ROM. The table is read by the channel change routine each time the channel is changed, and the data is sent to the PLL.

● **Method of serial data input to the PLL**

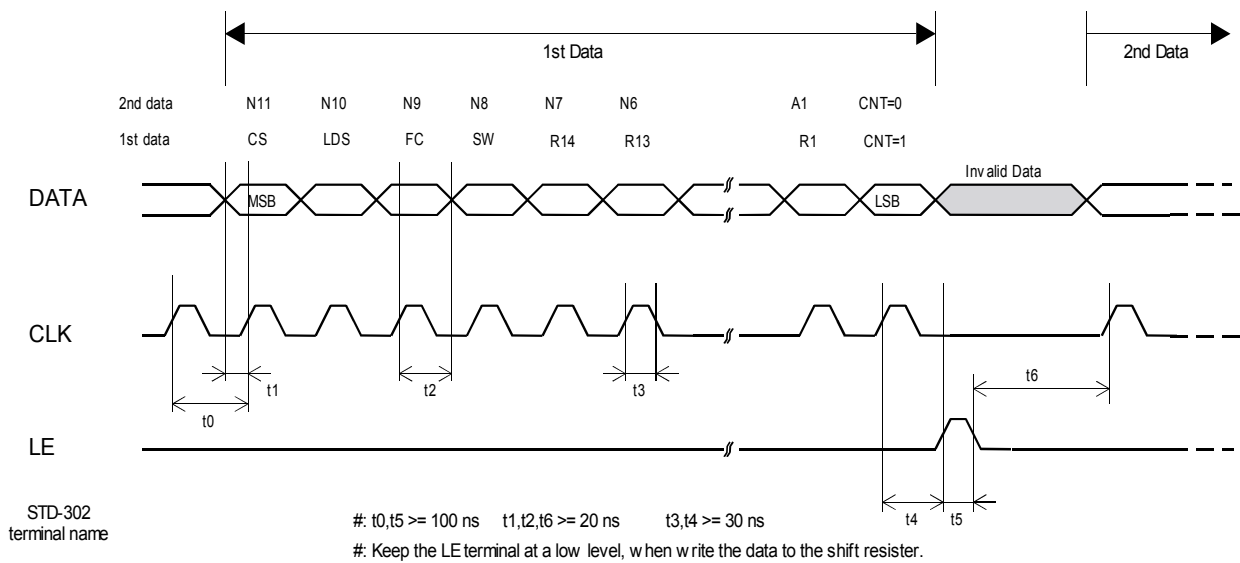
After the RF channel table plan is decided, the data needs to be allocated to the ROM table and read from there or calculated with the software.

Together with this setting data, operation bits that decide operation of the PLL must be sent to the PLL.

The operation bits for setting the PLL are as follows. These values are placed at the head of the reference counter value and are sent to the PLL.

1. CS: Charge pump current select bit
 CS = 0 +/-1.5 mA select VCO is optimized to +/-1.5 mA
2. LDS: LD/fout output setting bit
 LDS = 0 LD select Hardware is set to LD output
3. FC: Phase control bit for the phase comparator
 FC = 1 Hardware operates at this phase

Figure 2



The PLL IC, which operates as shown in the block diagram in the manual, shifts the data to the 19-bit shift register and then transfers it to the respective latch (counter, register) by judging the CNT control bit value input at the end.

1. CLK [Clock]: Data is shifted into the shift register on the rising edge of this clock.
2. LE [Load Enable]: Data in the 19-bit shift register is transferred to respective latches on the rising edge of the clock. The data is transferred to a latch according to the control bit CNT value.
3. Data [Serial Data]: You can perform either reference counter setup or programmable counter setup first.

TIMING CHART

Control timing in a typical application is shown in Figure 3.

Initial setting of the port connected to the radio module is performed when power is supplied by the CPU and reset is completed. MOS-FET for supply voltage control of the radio module, RXSEL and TXSEL are set to inactive to avoid unwanted emissions. The power supply of the radio module is then turned on. When the radio module is turned on, the PLL internal resistor is not yet set and the peripheral VCO circuit is unstable. Therefore data transmission and reception is possible 40 ms after the setting data is sent to the PLL at the first change of channel, however from the second change of channel, the circuit stabilizes within 20 ms and is able to handle the data.

Changing channels must be carried out in the receive mode. If switching is performed in transmission mode, unwanted emission occurs.

If the module is switched to the receive mode when operating in the same channel, (a new PLL setting is not necessary) it can receive data within 5 ms of switching^{*1}. For data transmission, if the RF channel to be used for transmission is set while still in receiving mode, data can be sent at 5 ms after the radio module is switched from reception to transmission^{*2}.

Check that the Lock Detect signal is "high" 20 ms after the channel is changed. In some cases the Lock Detect signal becomes unstable before the lock is correctly detected, so it is necessary to note if processing of the signal is interrupted. It is recommended to observe the actual waveform before writing the process program.

^{*1} DC offset may occur due to frequency drift caused by ambient temperature change. Under conditions below -10 °C, 10 to 20 ms delay of DO output is estimated. The customer is urged to verify operation at low temperature and optimize the timing.

^{*2} Sending '10101.....' preamble just after switching to transmission mode enables smoother operation of the binarization circuit of the receiver.

For 4800 bps, a preamble of '11001100' is effective.

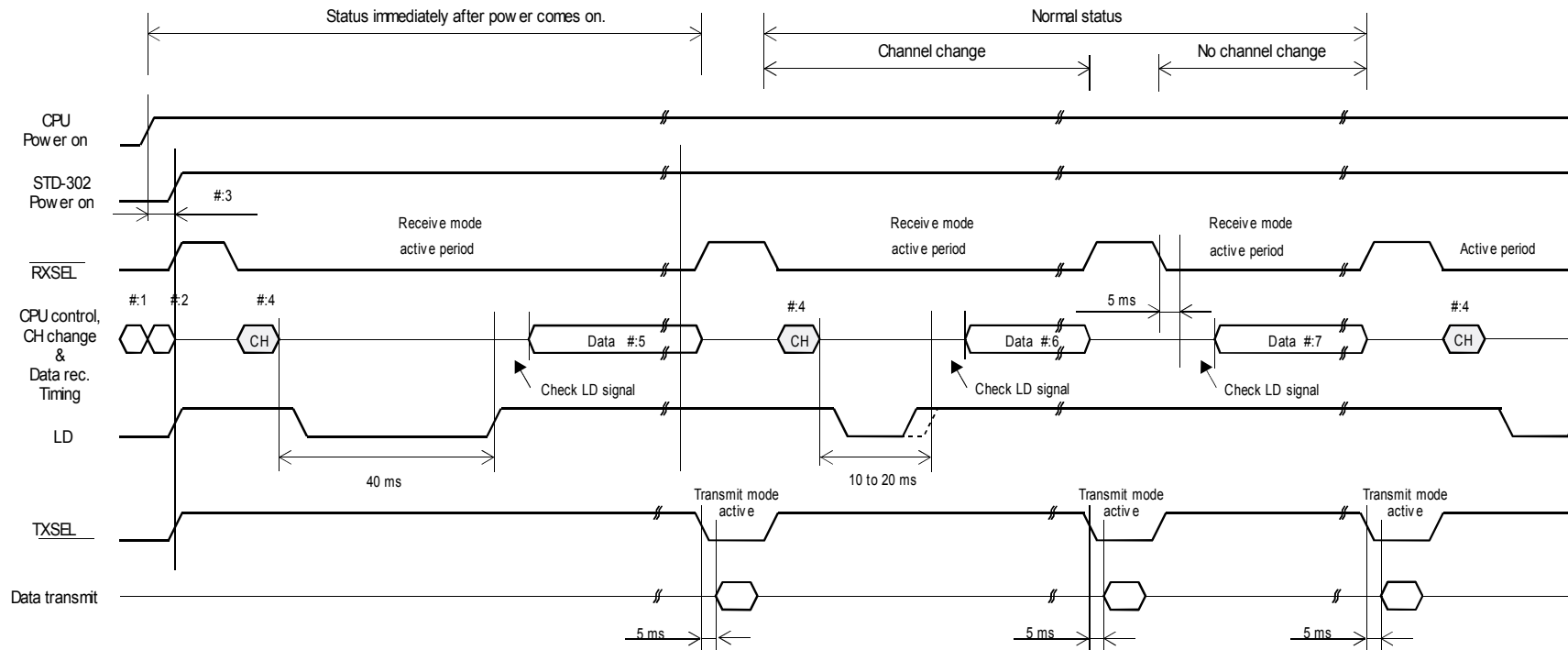
Recommended preamble length:

- 20 °C - + 60 °C : 20 ms

Remark

For details about PLL control and the sample programs, see our technical document 'STD-302 interface method'

Figure 3: Timing diagram for STD-302



- #1 Reset control CPU
- #2 Initialize the port connected to the module.
- #3 Supply power to the module after initializing CPU.
- #4 RFchannel change must be performed in receiving mode.

- #5 40 ms later, the receiver can receive the data after changing the channel..
- #6 10 to 20 ms later, the receiver can receive the data after changing the channel.
- #7 5 ms later, the data can be received if the RF channel is not changed.

PLL FREQUENCY SETTING DATA REFERENCE

335 MHz band (335.7125 – 335.8375 MHz)

Parameter name	Value
Phase Comparing Frequency F_{comp} [kHz]	25
Start Channel Frequency F_{ch} [MHz]	335.7125
Channel Step Frequency [kHz]	25
Number of Channel	6
Prescaler M	64

: For data input
 : Result of calculation
 : Fixed value

Parameter name	Value
Reference Frequency F_{osc} [MHz]	21.25
Offset Frequency F_{offset} [MHz]	21.7

Parameter name	Value
Reference Counter R	850
Programmable Counter N Min. Value	196
Programmable Counter N Max. Value	196
Swallow Counter A Min. Value	16
Swallow Counter A Max. Value	21

No.	Channel Frequency F_{CH}	Expect Frequency F_{EXPECT}	Lock Frequency F_{VCO}	Number of Division n	Programmable Counter N	Swallow Counter A
	(MHz)	(MHz)	(MHz)			
0	335.7125	314.0125	314.0000	12560	196	16
1	335.7375	314.0375	314.0250	12561	196	17
2	335.7625	314.0625	314.0500	12562	196	18
3	335.7875	314.0875	314.0750	12563	196	19
4	335.8125	314.1125	314.1000	12564	196	20
5	335.8375	314.1375	314.1250	12565	196	21

Regulatory compliance information

Compliance

STD-302N-R 335 MHz was designed to be installed in remote control systems used for cranes in India. The technical specifications referred to in the design phase are shown below:

Frequency	335.7125, 335.7375, 335.7625, 335.7875, 335.8125, 335.8375 MHz
Output power	≤ 1 mW
Band width	≤ 10 kHz

The relevant laws and regulations are subject to change.

Compliance assessment

This product was designed to meet the specification above, however it has not been assessed for conformity with the appropriate regulations. Users are required to verify that their final product meets the appropriate specifications and to perform the procedures for regulatory compliance.

Guarantee of regulatory compliance

We only guarantee that this product meets the specification in this document. We are exempt from any other responsibilities relating to regulatory compliance.

We also recommend that the user consults the authorities in the relevant country for detailed regulatory information such as valid regulations, test specifications, assessment procedures, marking methods etc, before starting any project with this product.

If technical documentation is required for compliance assessments, we will provide any documents, which may be considered necessary for assessment, under NDA. The documentation is only available in English.

Important notice

- Customers are advised to consult with Circuit Design sales representatives before ordering. Circuit Design believes the provided information is accurate and reliable. However, Circuit Design reserves the right to make changes to this product without notice.
- Circuit Design products are neither designed nor intended for use in life support applications where malfunction can reasonably be expected to result in significant personal injury to the user. Any use of Circuit Design products in such safety-critical applications is understood to be fully at the risk of the customer and the customer must fully indemnify Circuit Design, Inc for any damages resulting from any improper use.
- As the radio module communicates using electronic radio waves, there are cases where transmission will be temporarily cut off due to the surrounding environment and method of usage. The manufacturer is exempt from all responsibility relating to resulting harm to personnel or equipment and other secondary damage.
- The manufacturer is exempt from all responsibility relating to secondary damage resulting from the operation, performance and reliability of equipment connected to the radio module.

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Cautions

- Do not use the equipment within the vicinity of devices that may malfunction as a result of electronic radio waves from the radio module.
- Communication performance will be affected by the surrounding environment, so communication tests should be carried out before actual use.
- Ensure that the power supply for the radio module is within the specified rating. Short circuits and reverse connections may result in overheating and damage and must be avoided at all costs.
- Ensure that the power supply has been switched off before attempting any wiring work.
- The case is connected to the GND terminal of the internal circuit, so do not make contact between the '+' side of the power supply terminal and the case.
- When batteries are used as the power source, avoid short circuits, recharging, dismantling, and pressure. Failure to observe this caution may result in the outbreak of fire, overheating and damage to the equipment. Remove the batteries when the equipment is not to be used for a long period of time. Failure to observe this caution may result in battery leaks and damage to the equipment.
- Do not use this equipment in vehicles with the windows closed, in locations where it is subject to direct sunlight, or in locations with extremely high humidity.
- The radio module is neither waterproof nor splash proof. Ensure that it is not splashed with soot or water. Do not use the equipment if water or other foreign matter has entered the case.
- Do not drop the radio module or otherwise subject it to strong shocks.
- Do not subject the equipment to condensation (including moving it from cold locations to locations with a significant increase in temperature.)
- Do not use the equipment in locations where it is likely to be affected by acid, alkalis, organic agents or corrosive gas.
- Do not bend or break the antenna. Metallic objects placed in the vicinity of the antenna will have a great effect on communication performance. As far as possible, ensure that the equipment is placed well away from metallic objects.
- The GND for the radio module will also affect communication performance. If possible, ensure that the case GND and the circuit GND are connected to a large GND pattern.

Warnings

- Do not take apart or modify the equipment.
- Do not remove the product label (the label attached to the upper surface of the module.) Using a module from which the label has been removed is prohibited.

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REVISION HISTORY

Version	Date	Description	Remark
1.0	July 2010	STD-302N-R 335 MHz First issue	