UHF Narrow band radio transceiver

STD-302S 869MHz

Operation Guide

Version 2.0 (June 2017)

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GENERAL DESCRIPTION & FEATURES

General Description

The UHF FM narrow band semi-duplex radio data module STD-302S is a RED and RoHS compliant, high performance transceiver designed for use in industrial applications requiring long range, high performance and reliability.

All high frequency circuits are enclosed inside a robust housing to provide superior resistance against shock and vibration. The narrow band technique enables high interference rejection and concurrent operation with multiple modules.

STD-302S, a narrowband module with 25 kHz channel steps, achieves high TX/RX switching speed, making it an ideal RF unit for inclusion in feedback systems.

Features

- 5 mW RF power, 3.0 V operation
- Programmable RF channel
- Fast TX/RX switching time
- High sensitivity -116 dBm
- Excellent mechanical durability, high vibration & shock resistance
- RED (EN 300 220) / RoHS compliance

Applications

- Telemetry

  Water level monitor for rivers, dams, etc.
  Monitoring systems for environmental data such as temperature, humidity, etc.
  Transmission of measurement data (pressure, rpm, current, etc) to PC
  Security alarm monitoring
- Telecontrol

  Industrial remote control systems
  Remote control systems for factory automation machines
  Control of various driving motors
- Data transmission

  RS232/RS485 serial data transmission

SPECIFICATIONS

STD-302S 869 MHz

All ratings at 25 +/-10 °C unless otherwise noted

General characteristics

Item	Units	MIN	TYP	MAX	Remarks
Applicable standard			EN 300 220		
Communication method			Simplex, Half-duplex		
Emission class			F1D		
Operating frequency range	MHz	868		870	
Operation temperature range	°C	-20		60	No dew condensation
Storage temperature range	°C	-30		75	No dew condensation
Aging rate	ppm	-1		1	TX freq., RX Lo freq.
Initial frequency tolerance	ppm	-1.5		1.5	TX freq., RX Lo freq.
Dimensions	mm		30 x 50 x 9 mm		Not including antenna
Weight	g		25 g		

Electrical specification <Common>

Item		MIN	TYP	MAX	Remarks
Oscillation type			PLL controlled VCO		
Frequency stability (-10 to 55°C)	ppm	-3.4		3.4	Reference frequency at 25 °C
Frequency stability (-20 to 60°C)	ppm	-4		4	Reference frequency at 25 °C
TX/RX switching time	ms		15	20	DI/DO
Channel step	kHz		25		
Data rate	bps	2400		9600	DO/DI
Max. pulse width	ms			15	DO/DI
Min. pulse width	us	100			DO/DI
Data polarity			Positive		DO/DI
PLL reference frequency	MHz		21.25		TCXO
PLL response	ms		30	60	from PLL setting to LD out
Antenna impedance	Ω		50		Nominal
Operating voltage	V	3.0		5.5	
TX consumption current	mA		46	50	Vcc = 3.0 V
RX consumption current	mA		28	32	Vcc = 3.0 V

Transmitter part

Item		MIN	TYP	MAX	Remarks
RF output power	mW		5		Conducted 50 Ω
Deviation	kHz	2.35	2.75	3.15	PN9 9600 bps
DI input level	V	0		5.5	L= GND, H = 3 V- Vcc
Residual FM noise	kHz		0.35		DI=L, LPF=20 kHz
Spurious emission	dBm			-54	47-74, 87.5-118, 174-230, 470-862 MHz
				-36	Other frequencies below 1000 MHz
				-30	Frequencies above 1000 MHz
Adjacent CH power	dBm			-37	PN9 9600 bps CH25kHz/BW16kHz

Receiver part

Item		MIN	TYP	MAX	Remarks
Receiver type		Double superheterodyne			
1st IF frequency	MHz		21.7		
2nd IF frequency	kHz		450		
Maximum input level	dBm			10	
BER (0 error/2556 bits) *1	dBm	-104	-107		At 869MHz PN 9 9600bps
BER (1 % error) *2	dBm		-113		At 869MHz PN 9 9600bps
Sensitivity 12dB/ SINAD	dBm		-116		fm1 k/ dev 2.75 kHz CCITT
Spurious response rejection *3	dB		60		1 st Mix, 2 signal method, 1 % error
			60		2 nd Mix, 2 signal method, 1 % error
Adjacent CH selectivity *3	dB		45		+/- 25 kHz, 2 signal method, 1 % error
Intermodulation *4	dB		50		2 signal method, 1 % error
DO output level	V	0		2.8	L = GND H = 2.8 V
RSSI rising time	ms		30	50	CH shift of 25 kHz (from PLL setup)
			50	70	When power ON (from PLL setup)
Time until valid Data-out *5	ms		50	100	CH shift of 25 kHz (from PLL setup)
			70	120	When power ON (from PLL setup)
Spurious radiation	dBm		-60	-57	Below 1000 MHz
			-60	-47	Above 1000 MHz
RSSI	mV	120	170	220	With -113 dBm at 869MHz

Specifications are subject to change without prior notice

Notice

- The time required until a stable DO is established may get longer due to the possible frequency drift caused by operation environment changes, especially when switching from TX to RX, from RX to TX and changing channels. Please make sure to optimize the timing. The recommended preamble is more than 20 ms.
- Antenna connection is designed as pin connection.
- RF output power, sensitivity, spurious emission and spurious radiation levels may vary with the trace used between the RF pin and the coaxial connection. Please make sure to verify those parameters before use.
- The feet of the shield case should be soldered to the wide GND pattern to avoid any change in characteristics.

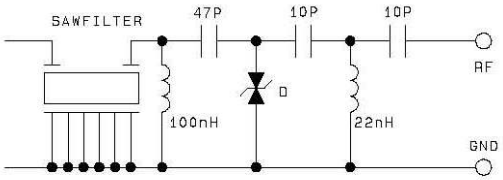
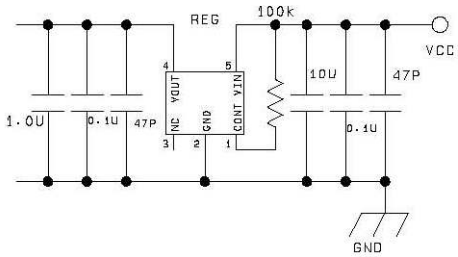
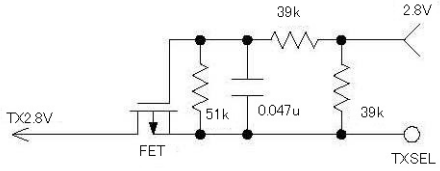
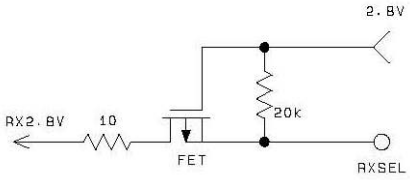
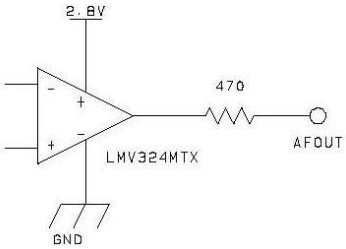
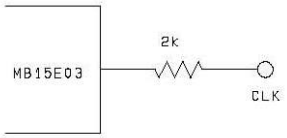
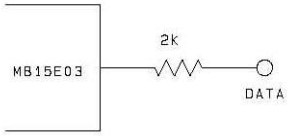
Notes about the specification values

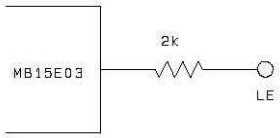
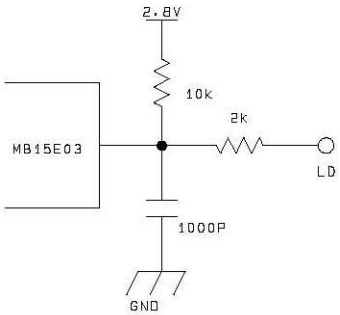
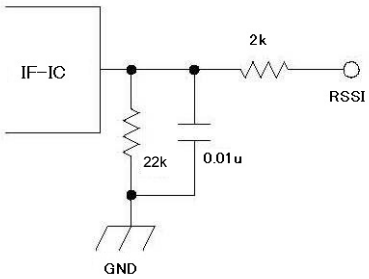
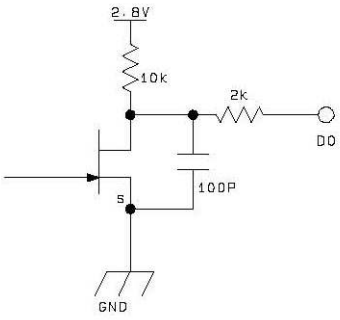
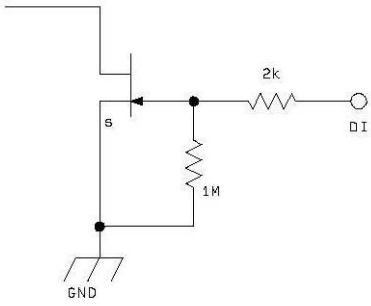
*1 BER: RF level where no error per 2556 bits is confirmed with the signal of PN9 and 9600 bps.
*2 BER (1 % error) : RF level where 1% error per 2556 bits is confirmed with the signal of PN9 and 9600 bps.
*3 Spurious response, CH selectivity: Jamming signal used in the measurement is unmodulated.
*4 Intermodulation: Ratio between the receiver input level with BER 1% and the signal level (PN9 9600 bps) added at the points of 'Receiving frequency - 200 kHz ' + ' Receiving frequency -100kHz' with which BER 1% is achieved.
*5 Time until valid Data-out : Valid DO is determined at the point where Bit Error Rate meter starts detecting the signal of 9600bps, 1010repeated signal.

All specifications are specified based on the data measured in a shield room using the PLL setting controller board prepared by Circuit Design.

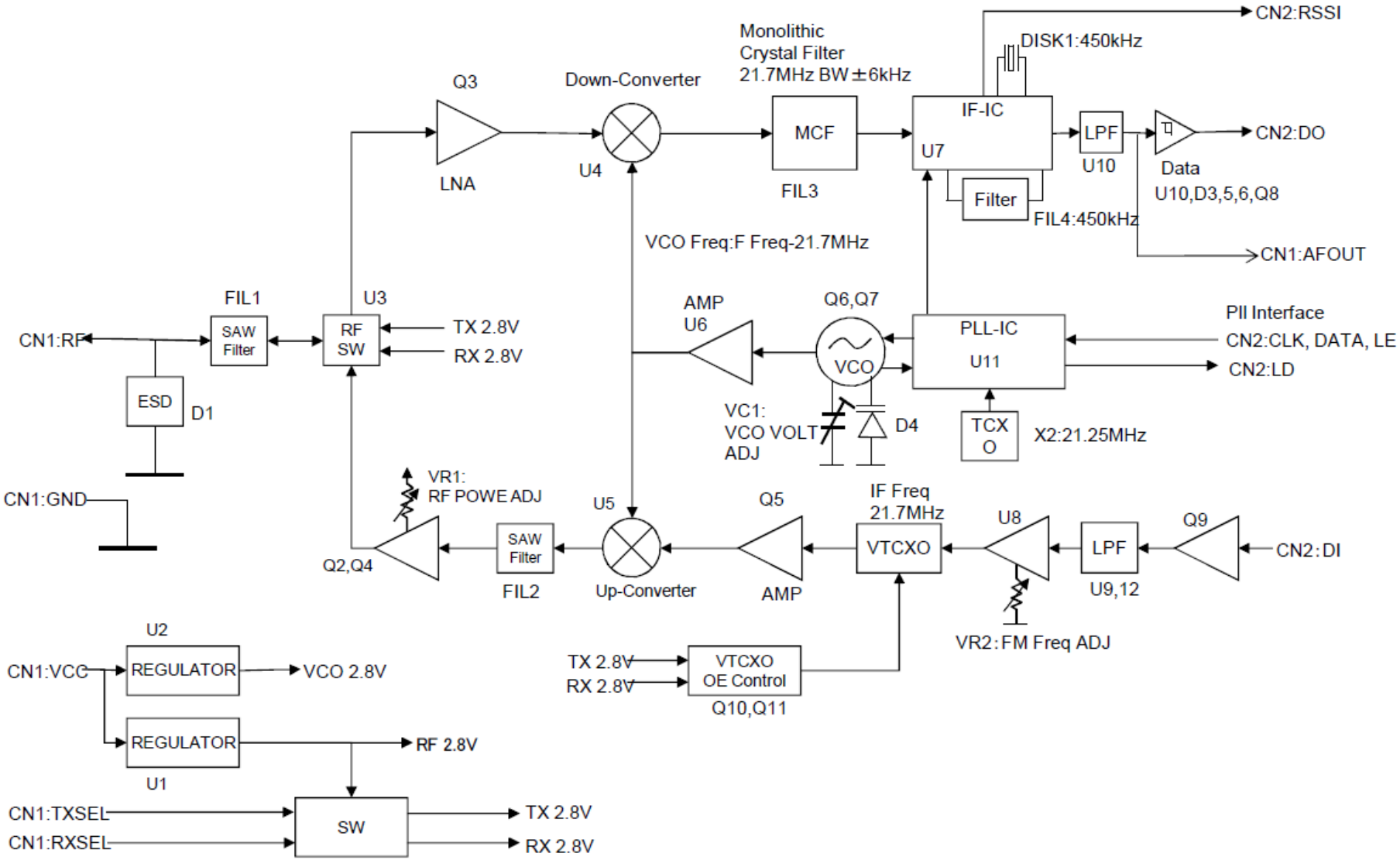
Measuring equipment:
SG=ANRITUS communication analyzer MT2605
Spectrum analyzer = ANRITSU MS2663G
BER measure = ANRITSU MP1201G

PIN DESCRIPTION

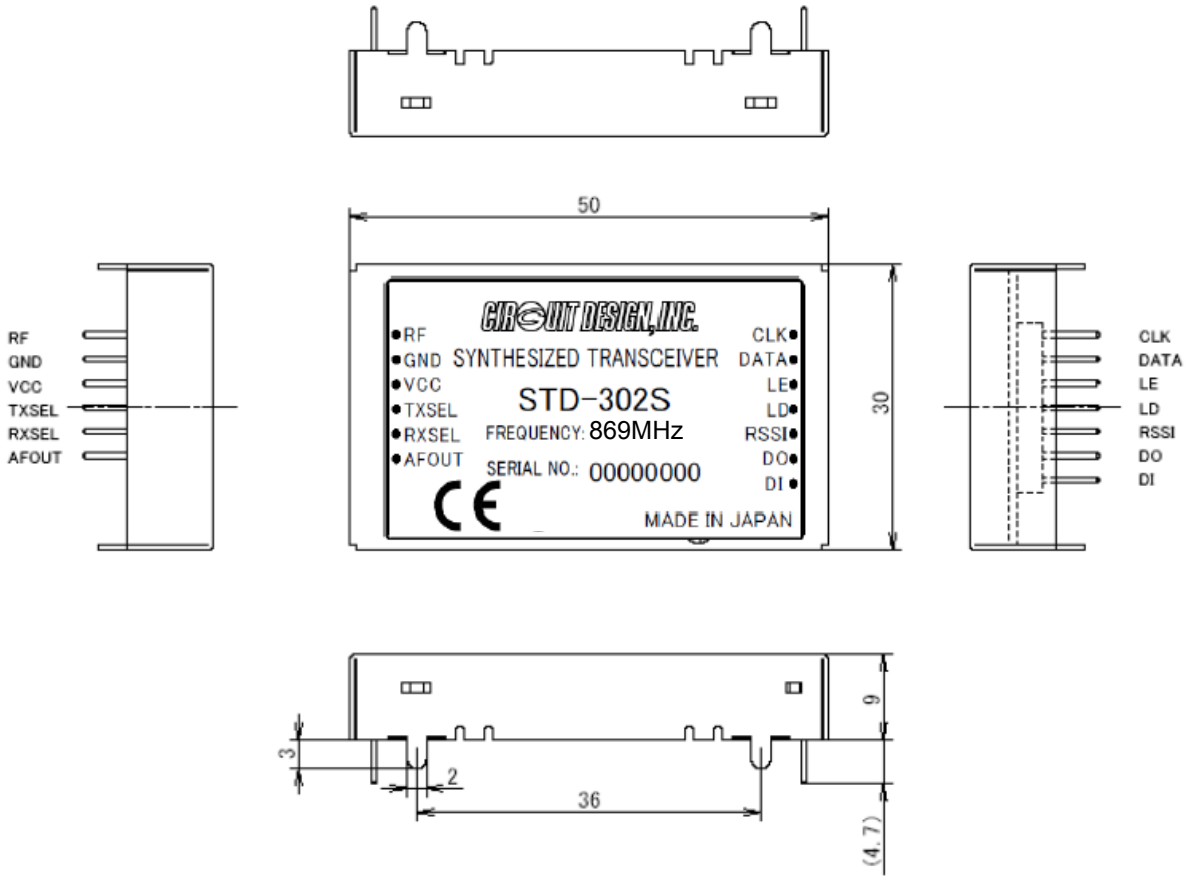
Pin name	I/O	Description	Equivalent circuit
RF	I/O	RF input terminal Antenna impedance nominal 50 **Ω**	
GND	I	GROUND terminal The GND pins and the feet of the shield case should be connected to the wide GND plane.	
VCC	I	Power supply terminal DC 3.0 to 5.5 V	
TXSEL	I	TX select terminal GND = TXSEL active To enable the transmitter circuits, connect TXSEL to GND and RXSEL to OPEN or 2.8 V.	
RXSEL	I	RX select terminal GND= RXSEL active To enable the receiver circuits, connect RXSEL to GND and TXSEL to OPEN or 2.8 V.	
AF	O	Analogue output terminal There is DC offset of approx. 1 V. Refer to the specification table for amplitude level.	
CLK	I	PLL data setting input terminal Interface voltage H = 2.8 V, L = 0 V	
DATA	I	PLL data setting input terminal Interface voltage H = 2.8 V, L = 0 V	

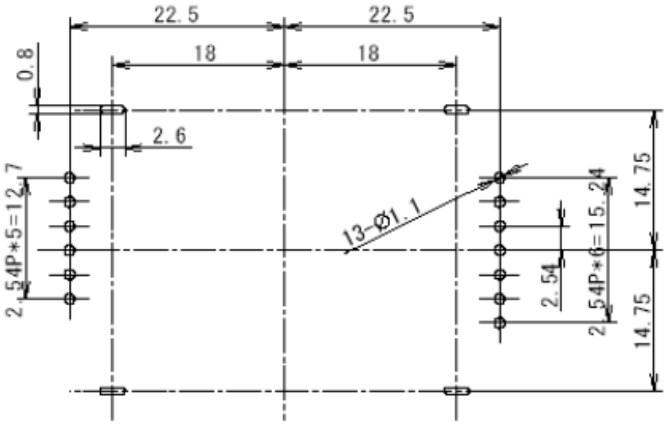
LE	I	Load enable signal input terminal for PLL data setting input Interface voltage H = 2.8 V, L = 0 V	
LD	O	PLL lock/unlock indicator terminal Lock = H (2.8 V), Unlock = L (0 V)	
RSSI	O	Received Signal Strength Indicator terminal	
DO	O	Data output terminal Interface voltage: H=2.8V, L=0V	
DI	I	Data input terminal Interface voltage: H=2.8V to Vcc, L=0V Input data pulse width Min.100 µs Max. 15 ms	

BLOCK DIAGRAM <STD-302S 869MHz>



DIMENSIONS



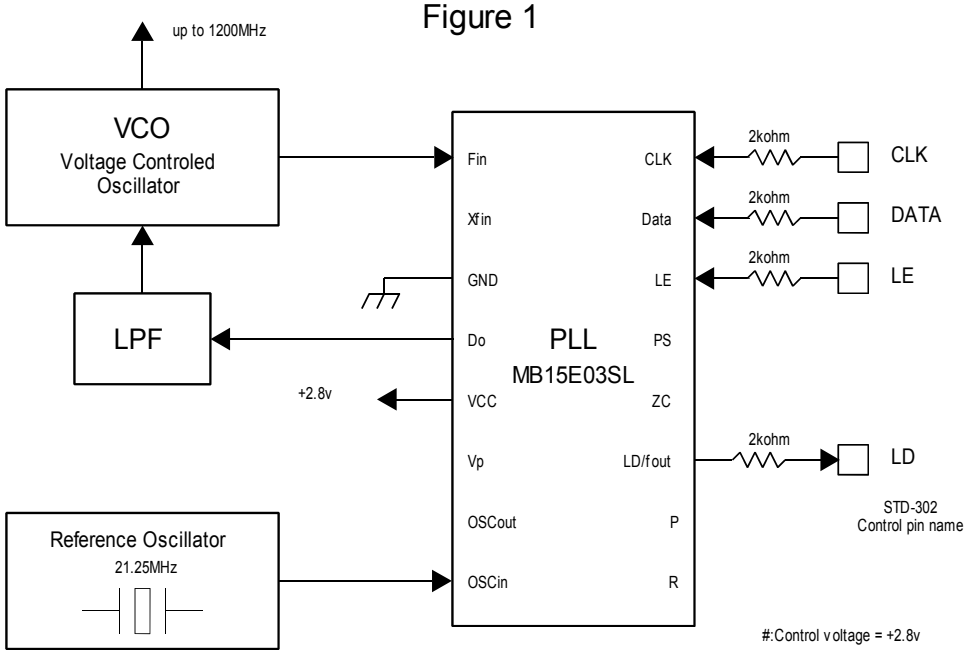


Reference hole position for PCB mounting(Top view)

PLL IC CONTROL

- **PLL IC control**

Figure 1



STD-302S is equipped with an internal PLL frequency synthesizer as shown in Figure 1. The operation of the PLL circuit enables the VCO to oscillate at a stable frequency. Transmission frequency is set externally by the controlling IC. STD-302S has control terminals (CLK, LE, DATA) for the PLL IC and the setting data is sent to the internal register serially via the data line. Also STD-302S has a Lock Detect (LD) terminal that shows the lock status of the frequency. These signal lines are connected directly to the PLL IC through a 2 kΩ resistor.

The interface voltage of STD-302S is 2.8 V, so the control voltage must be the same.
STD-302S comes equipped with a Fujitsu MB15E03SL PLL IC. Please refer to the manual of the PLL IC.

The following is a supplementary description related to operation with STD-302S. In this description, the same names and terminology as in the PLL IC manual are used, so please read the manual beforehand.

- **How to calculate the setting values for the PLL register**

The PLL IC manual shows that the PLL frequency setting value is obtained with the following equation.

$f_{vco} = [(M \times N)+A] \times f_{osc} / R$ -- Equation 1

f_{vco} : Output frequency of external VCO
M: Preset divide ratio of the prescaler (64 or 128)
N: Preset divide ratio of binary 11-bit programmable counter (3 to 2,047)
A: Preset divide ratio of binary 7-bit swallow counter ($0 \le A \le 127$ A<N))
f_{osc}: Output frequency of the reference frequency oscillator
R: Preset divide ratio of binary 14-bit programmable reference counter (3 to 16,383)

With STD-302S, there is an offset frequency (f_{offset}) 21.7 MHz for the transmission RF channel frequency f_{ch}. Therefore the expected value of the frequency generated at VCO (f_{expect}) is as below.

$f_{vco} = f_{expect} = f_{ch} – f_{offset}$ ---- Equation 2

The PLL internal circuit compares the phase to the oscillation frequency $f_{vco.}$ This phase comparison frequency (f_{comp}) must be decided. f_{comp} is made by dividing the frequency input to the PLL from the reference frequency oscillator by reference counter R. STD-302S uses 21.25 MHz for the reference clock $f_{osc.}$ f_{comp} is one of 6.25 kHz, 12.5 kHz or 25 kHz.

The above equation 1 results in the following with n = M x N + A, where “n” is the number for division.

$f_{vco}=n*f_{comp}$ ---- Equation 3 $n = f_{vco}/f_{comp}$ ---- Equation 4 note: $f_{comp} = f_{osc}/R$

Also, this PLL IC operates with the following R, N, A and M relational expressions.

$R=f_{osc}/f_{comp}$ ---- Equation 5 N = INT (n / M) ---- Equation 6 A = n - (M x N) ---- Equation 7
INT: integer portion of a division.

As an example, the setting value of RF channel frequency f_{ch} 869.725 MHz can be calculated as below.
The constant values depend on the electronic circuits of STD-302S.

Conditions: Channel center frequency: f_{ch} = 869.725 MHz
Constant: Offset frequency: f_{offset}=21.7 MHz
Constant: Reference frequency: f_{osc}=21.25 MHz
Set 25 kHz for Phase comparison frequency and 64 for Prescaler value M

The frequency of VCO will be

$f_{vco} = f_{expect} = f_{ch} - f_{offset}$ = 869.725 –21.7 = 848.025MHz

Dividing value “n” is derived from Equation 4

$n = f_{vco} / f_{comp}$ = 848.025MHz/25kHz = 33921

Value “R” of the reference counter is derived from Equation 5.

$R = f_{osc}/f_{comp}$ = 21.25MHz/25kHz = 850

Value “N” of the programmable counter is derived from Equation 6.

N = INT (n/M) = INT(33921/64) = 530

Value “A“ of the swallow counter is derived from Equation 7.

A = n – (M x N) = 33921 – 64 x 530 = 1

The frequency of STD-302S is locked at a center frequency f_{ch} by inputting the PLL setting values N, A and R obtained with the above equations as serial data. The above calculations are the same for the other frequencies.
Excel sheets that contain automatic calculations for the above equations can be found on our web site (www.cdt21.com/).

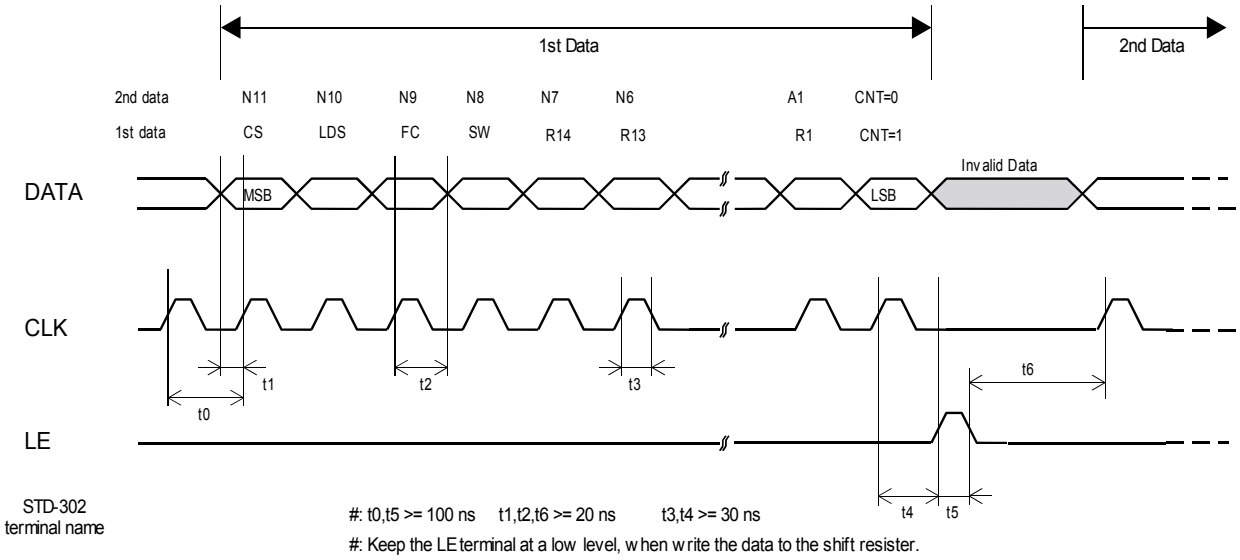
The result of the calculations is arranged as a table in the CPU ROM. The table is read by the channel change routine each time the channel is changed, and the data is sent to the PLL.

- **Method of serial data input to the PLL**

After the RF channel table plan is decided, the data needs to be allocated to the ROM table and read from there or calculated with the software.
Together with this setting data, operation bits that decide operation of the PLL must be sent to the PLL.
The operation bits for setting the PLL are as follows. These values are placed at the head of the reference counter value and are sent to the PLL.

1. CS: Charge pump current select bit
   CS = 0 +/-1.5 mA select VCO is optimized to +/-1.5 mA
2. LDS: LD/fout output setting bit
   LDS = 0 LD select Hardware is set to LD output
3. FC: Phase control bit for the phase comparator
   FC = 1 Hardware operates at this phase

Figure 2



The PLL IC, which operates as shown in the block diagram in the manual, shifts the data to the 19-bit shift register and then transfers it to the respective latch (counter, register) by judging the CNT control bit value input at the end.

1. CLK [Clock]: Data is shifted into the shift register on the rising edge of this clock.
2. LE [Load Enable]: Data in the 19-bit shift register is transferred to respective latches on the rising edge of the clock. The data is transferred to a latch according to the control bit CNT value.
3. Data [Serial Data]: You can perform either reference counter setup or programmable counter setup first.

TIMING CHART

Control timing in a typical application is shown in Figure 3.
Initial setting of the port connected to the radio module is performed when power is supplied by the CPU and reset is completed. MOS-FET for supply voltage control of the radio module, RXSEL and TXSEL are set to inactive to avoid unwanted emissions. The power supply of the radio module is then turned on. When the radio module is turned on, the PLL internal resistor is not yet set and the peripheral VCO circuit is unstable. Therefore data transmission and reception is possible 40 ms after the setting data is sent to the PLL at the first change of channel, however from the second change of channel, the circuit stabilizes within 20 ms and is able to handle the data.
Changing channels must be carried out in the receive mode. If switching is performed in transmission mode, unwanted emission occurs.

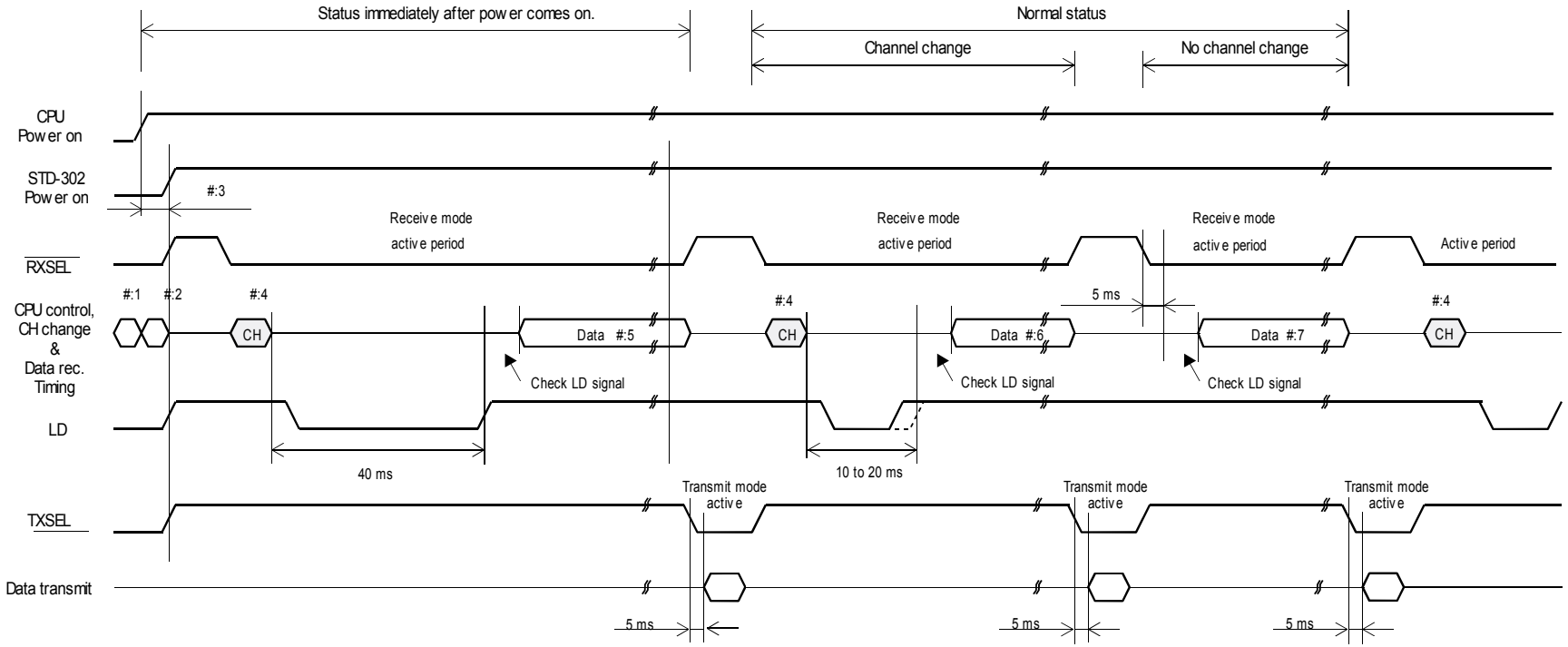
If the module is switched to the receive mode when operating in the same channel, (a new PLL setting is not necessary) it can receive data within 5 ms of switching[*1]. For data transmission, if the RF channel to be used for transmission is set while still in receiving mode, data can be sent at 5 ms after the radio module is switched from reception to transmission[*2].
Check that the Lock Detect signal is “high” 20 ms after the channel is changed. In some cases the Lock Detect signal becomes unstable before the lock is correctly detected, so it is necessary to note if processing of the signal is interrupted. It is recommended to observe the actual waveform before writing the process program.

[*1] DC offset may occur due to frequency drift caused by ambient temperature change. Under conditions below -10 °C, 10 to 20 ms delay of DO output is estimated. The customer is urged to verify operation at low temperature and optimize the timing.

[*2] Sending ‘10101…..’ preamble just after switching to transmission mode enables smoother operation of the binarization circuit of the receiver. For 9600 bps, a preamble of ‘11001100’ is effective.

Remark
For details about PLL control and the sample programs, see our technical document ‘STD-302 interface method’

Figure 3: Timing diagram for STD-302



#:1 Reset control CPU
#:2 Initialize the port connected to the module.
#:3 Supply power to the module after initializing CPU.
#:4 RFchannel change must be performed in receiving mode.
#:5 40 ms later, the receiver can receive the data after changing the channel..
#:6 10 to 20 ms later, the receiver can receive the data after changing the channel.
#:7 5 ms later, the data can be received if the RF channel is not changed.

PLL FREQUENCY SETTING DATA REFERENCE

869MHz band (868 – 870MHz)

Parameter name	Value
Phase Comparing Frequency FCOMP [kHz]	25
Start Channel Frequency FCH [MHz]	868.025
Channel Step Frequency [kHz]	25
Number of Channel	79
Prescaler M	64

: For data input
: Result of calculation
: Fixed value

Parameter name	Value
Reference Frequency FOSC [MHz]	21.25
Offset Frequency FOFFSET [MHz]	21.7

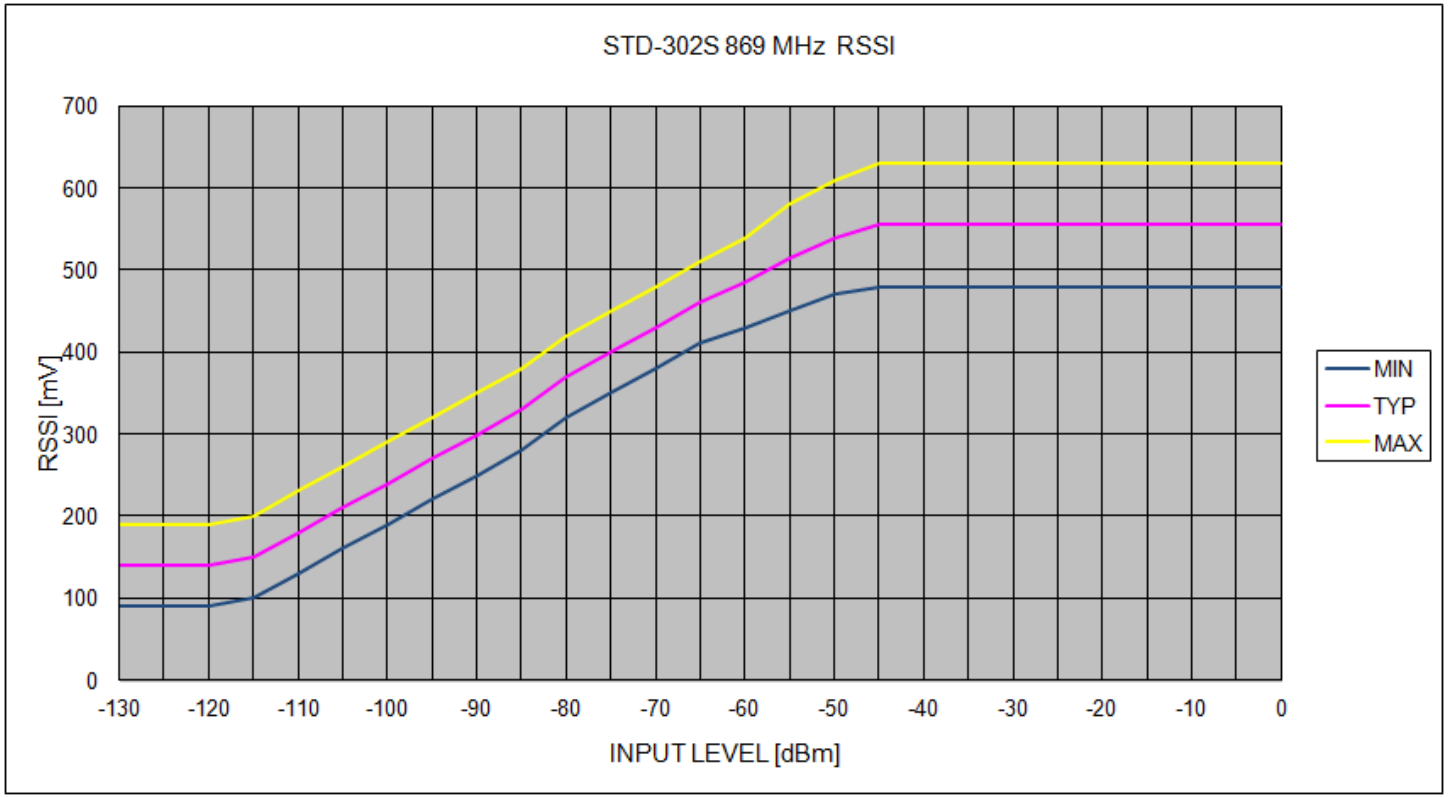
Parameter name	Value
Reference Counter R	850
Programmable Counter N Min. Value	528
Programmable Counter N Max. Value	530
Swallow Counter A Min. Value	0
Swallow Counter A Max. Value	63

No.	Channel Frequency FCH (MHz)	Expect Frequency FEXPECT (MHz)	Lock Frequency FVCO (MHz)	Number of Division n	Programmable Counter N	Swallow Counter A
0	868.0250	846.3250	846.3250	33853	528	61
1	868.0500	846.3500	846.3500	33854	528	62
2	868.0750	846.3750	846.3750	33855	528	63
3	868.1000	846.4000	846.4000	33856	529	0
4	868.1250	846.4250	846.4250	33857	529	1
5	868.1500	846.4500	846.4500	33858	529	2
6	868.1750	846.4750	846.4750	33859	529	3
7	868.2000	846.5000	846.5000	33860	529	4
8	868.2250	846.5250	846.5250	33861	529	5
9	868.2500	846.5500	846.5500	33862	529	6
10	868.2750	846.5750	846.5750	33863	529	7
11	868.3000	846.6000	846.6000	33864	529	8
12	868.3250	846.6250	846.6250	33865	529	9
13	868.3500	846.6500	846.6500	33866	529	10
14	868.3750	846.6750	846.6750	33867	529	11
15	868.4000	846.7000	846.7000	33868	529	12
16	868.4250	846.7250	846.7250	33869	529	13
17	868.4500	846.7500	846.7500	33870	529	14
18	868.4750	846.7750	846.7750	33871	529	15
19	868.5000	846.8000	846.8000	33872	529	16
20	868.5250	846.8250	846.8250	33873	529	17
21	868.5500	846.8500	846.8500	33874	529	18
22	868.5750	846.8750	846.8750	33875	529	19
23	868.6000	846.9000	846.9000	33876	529	20
24	868.6250	846.9250	846.9250	33877	529	21
25	868.6500	846.9500	846.9500	33878	529	22
26	868.6750	846.9750	846.9750	33879	529	23
27	868.7000	847.0000	847.0000	33880	529	24
28	868.7250	847.0250	847.0250	33881	529	25
29	868.7500	847.0500	847.0500	33882	529	26
30	868.7750	847.0750	847.0750	33883	529	27
31	868.8000	847.1000	847.1000	33884	529	28
32	868.8250	847.1250	847.1250	33885	529	29

33	868.8500	847.1500	847.1500	33886	529	30
34	868.8750	847.1750	847.1750	33887	529	31
35	868.9000	847.2000	847.2000	33888	529	32
36	868.9250	847.2250	847.2250	33889	529	33
37	868.9500	847.2500	847.2500	33890	529	34
38	868.9750	847.2750	847.2750	33891	529	35
39	869.0000	847.3000	847.3000	33892	529	36
40	869.0250	847.3250	847.3250	33893	529	37
41	869.0500	847.3500	847.3500	33894	529	38
42	869.0750	847.3750	847.3750	33895	529	39
43	869.1000	847.4000	847.4000	33896	529	40
44	869.1250	847.4250	847.4250	33897	529	41
45	869.1500	847.4500	847.4500	33898	529	42
46	869.1750	847.4750	847.4750	33899	529	43
47	869.2000	847.5000	847.5000	33900	529	44
48	869.2250	847.5250	847.5250	33901	529	45
49	869.2500	847.5500	847.5500	33902	529	46
50	869.2750	847.5750	847.5750	33903	529	47
51	869.3000	847.6000	847.6000	33904	529	48
52	869.3250	847.6250	847.6250	33905	529	49
53	869.3500	847.6500	847.6500	33906	529	50
54	869.3750	847.6750	847.6750	33907	529	51
55	869.4000	847.7000	847.7000	33908	529	52
56	869.4250	847.7250	847.7250	33909	529	53
57	869.4500	847.7500	847.7500	33910	529	54
58	869.4750	847.7750	847.7750	33911	529	55
59	869.5000	847.8000	847.8000	33912	529	56
60	869.5250	847.8250	847.8250	33913	529	57
61	869.5500	847.8500	847.8500	33914	529	58
62	869.5750	847.8750	847.8750	33915	529	59
63	869.6000	847.9000	847.9000	33916	529	60
64	869.6250	847.9250	847.9250	33917	529	61
65	869.6500	847.9500	847.9500	33918	529	62
66	869.6750	847.9750	847.9750	33919	529	63
67	869.7000	848.0000	848.0000	33920	530	0
68	869.7250	848.0250	848.0250	33921	530	1
69	869.7500	848.0500	848.0500	33922	530	2
70	869.7750	848.0750	848.0750	33923	530	3
71	869.8000	848.1000	848.1000	33924	530	4
72	869.8250	848.1250	848.1250	33925	530	5
73	869.8500	848.1500	848.1500	33926	530	6
74	869.8750	848.1750	848.1750	33927	530	7
75	869.9000	848.2000	848.2000	33928	530	8
76	869.9250	848.2250	848.2250	33929	530	9
77	869.9500	848.2500	848.2500	33930	530	10
78	869.9750	848.2750	848.2750	33931	530	11

TEST DATA

RSSI typical output level characteristic / Measurement frequency: 869 MHz / Modulation: unmodulated / 25°C +/- 5°C



Measurement was performed with the PLL setting control board prepared by Circuit Design.

INPUT LEVEL	RSSI		
	MIN	TYP	MAX
-130	90	140	190
-125	90	140	190
-120	90	140	190
-115	100	150	200
-110	130	180	230
-105	160	210	260
-100	190	240	290
-95	220	270	320
-90	250	300	350
-85	280	330	380
-80	320	370	420
-75	350	400	450
-70	380	430	480
-65	410	460	510
-60	430	485	540
-55	450	515	580
-50	470	540	610
-45	480	555	630
-40	480	555	630
-35	480	555	630
-30	480	555	630
-25	480	555	630
-20	480	555	630
-15	480	555	630
-10	480	555	630
-5	480	555	630
0	480	555	630

Regulatory compliance information

Declaration of Conformity

Hereby, Circuit Design, Inc. declares that the STD-302S is in compliance with RE Directive (2014/53/EU).
The full text of the EU Declaration of Conformity is available at www.circuitdesign.jp.

Cautions related to regulatory compliance when embedding the STD-302S

1. Duty cycle

The STD-302S is designed to be used in the EU wide harmonised frequency bands for shor range devices. The STD-302S continuously emits carrier signals when power is supplied. The user must design the final product to meet the relevant duty cycle requirement (For more detais, refer to the EN300 220-2).

2. Antenna

The STD-302S is supplied without a dedicated antenna.

The conformity assessment of the STD-302S (869 MHz) was performed using Circuit Design's standard antenna ANT-LEA-02(1/4 lambda lead antenna), so we recommend using the ANT-LEA-02 antenna or an antenna with equivalent characteristics (2.14 dBi or less). For details about our standard antenna, refer to www.circuitdesign.jp or contact us. If you use an antenna other than the recommended antenna, further radio conformity assessment may be required.

3. Supply voltage

The STD-302S should be used within the specified voltage range (3.0 V to 5.5 V).

4. Enclosure

To fulfill the requirements of EMC and safety requirements, the STD-302S should be mounted on the circuit board of the final product and must be enclosed in the case of the final product. No surface of the STD-302S should be exposed.

Conformity assessment of the final product

The manufacturer of the final system needs to conduct full EMC testing in the final configuration and also ensure the final product fulfills the safety requirements and is also responsible for the conformity assessment procedures of the final product in accordance with the RE Directive.

Important notice

- Customers are advised to consult with Circuit Design sales representatives before ordering.
  Circuit Design believes the provided information is accurate and reliable. However, Circuit Design reserves the right to make changes to this product without notice.
- Circuit Design products are neither designed nor intended for use in life support applications where malfunction can reasonably be expected to result in significant personal injury to the user. Any use of Circuit Design products in such safety-critical applications is understood to be fully at the risk of the customer and the customer must fully indemnify Circuit Design, Inc for any damages resulting from any improper use.
- As the radio module communicates using electronic radio waves, there are cases where transmission will be temporarily cut off due to the surrounding environment and method of usage. The manufacturer is exempt from all responsibility relating to resulting harm to personnel or equipment and other secondary damage.
- The manufacturer is exempt from all responsibility relating to secondary damage resulting from the operation, performance and reliability of equipment connected to the radio module.

Cautions

- As the radio module communicates using electronic radio waves, there are cases where transmission will be temporarily cut off due to the surrounding environment and method of usage. The manufacturer is exempt from all responsibility relating to resulting harm to personnel or equipment and other secondary damage.
- Do not use the equipment within the vicinity of devices that may malfunction as a result of electronic radio waves from the radio module.
- The manufacturer is exempt from all responsibility relating to secondary damage resulting from the operation, performance and reliability of equipment connected to the radio module.
- Communication performance will be affected by the surrounding environment, so communication tests should be carried out before actual use.
- Ensure that the power supply for the radio module is within the specified rating. Short circuits and reverse connections may result in overheating and damage and must be avoided at all costs.
- Ensure that the power supply has been switched off before attempting any wiring work.
- The case is connected to the GND terminal of the internal circuit, so do not make contact between the '+' side of the power supply terminal and the case.
- When batteries are used as the power source, avoid short circuits, recharging, dismantling, and pressure. Failure to observe this caution may result in the outbreak of fire, overheating and damage to the equipment. Remove the batteries when the equipment is not to be used for a long period of time. Failure to observe this caution may result in battery leaks and damage to the equipment.
- Do not use this equipment in vehicles with the windows closed, in locations where it is subject to direct sunlight, or in locations with extremely high humidity.
- The radio module is neither waterproof nor splash proof. Ensure that it is not splashed with soot or water. Do not use the equipment if water or other foreign matter has entered the case.
- Do not drop the radio module or otherwise subject it to strong shocks.
- Do not subject the equipment to condensation (including moving it from cold locations to locations with a significant increase in temperature.)
- Do not use the equipment in locations where it is likely to be affected by acid, alkalis, organic agents or corrosive gas.
- Do not bend or break the antenna. Metallic objects placed in the vicinity of the antenna will have a great effect on communication performance. As far as possible, ensure that the equipment is placed well away from metallic objects.
- The GND for the radio module will also affect communication performance. If possible, ensure that the case GND and the circuit GND are connected to a large GND pattern.

Warnings

- Do not take apart or modify the equipment.
- Do not remove the product label (the label attached to the upper surface of the module.) Using a module from which the label has been removed is prohibited.

REVISION HISTORY

Version	Date	Description	Remark
1.0	Oct.2015	The first issue	
1.1	Dec.2015	RSSI characteristics updated	
2.0	June 2017	Update according to RED requirements	